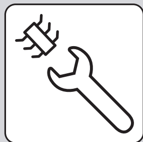
PROJECT RESULT



Technology platform for next-generation core CMOS process

2A704: Robust design for efficient use of nanometre technologies

Making chip designs more robust

Integrated circuit designers have all too often had to compromise on expected performance levels for their chip designs because of physical weaknesses appearing at the design verification or production level. Leading European chipmakers, circuit developers and design automation equipment manufacturers worked together under the umbrella of the MEDEA+ ROBIN project to tackle such problems earlier in the design phase and to improve design methods. New design flows leading to more robust circuits have given an important boost to the whole of the European semiconductor design and manufacturing sector.

Designers of high-speed chips have had to build redundancy into designs to allow for the imperfect environments of production and use that vary from the ideal of the 'designers' workbench'. Issues such as voltage variations, thermal heat effects, electrostatic discharge (ESD), internal radiation and crosstalk can all downgrade the performance and reliability of a perfect design.

With circuit detail resolutions now descending to 65 and 45 nm, such problems are becoming more acute. All too often, chip designs pass traditional verification checks, yet fail when manufactured in silicon, forcing design teams to turn to costly diagnostic and repair methods or – still worse – to throw the chip away.

If such issues can be defined and dealt with earlier in the design phase, problems further down the development flow can be avoided, as can production compromises that reduce final performance. This is why three major European chipmakers – Infineon, NXP Semiconductors and STMicroelectronics – got together in the MEDEA+ 2A704 ROBIN project to research how to tackle these issues early in the design phase.

Reliability and performance

The partners aimed to optimise their design approach to both existing 130 and 90 nm and future 65 and 45 nm technologies by defining the most efficient trade-offs between circuit robustness in terms of yield and reliability, and efficient use of technology affecting performance, density and power consumption. They were joined by a laboratory with strong expertise in quantum physics and four electronic design automation (EDA) companies.

The challenge was to maintain or enhance existing performance levels, while improving design reliability and robustness. Following a bottom-up approach, from technology to chip level and then to system-in-package (SIP) level, ROBIN examined a wide range of issues, from power and substrate effects through signal interference to manufacturing cost.

Its objective was to find better ways to overcome two typical design failings:

1. **Under design** – through considering the physical effects too late in the design flow; or
2. **Over design** – by overcompensating for likely performance downgrades when in production.

The focus was on mixed-mode chips that host both digital and analogue blocks.

Much of the project focused on enhancing designer expertise in analogue circuit theory, building simulation models, developing test structures, defining go/no-go flags and deriving design rules to ensure reliable chip functioning in production.

In the final phase, the software tools were brought up to production level, the models

refined and the design flows and measurement techniques – on- and off-chip – validated for production use. These final steps were mainly at the 65/45 nm technology level.

Developing robust designs

ROBIN achieved significant advances, especially in design robustness. The most important were a 50% improvement in ESD resistance from 500 to 750 V and a 25 dB reduction in cross talk from digital to analogue – significant steps to building design stability in use. These were achieved at no cost in terms of power consumption – in fact new design techniques for on-chip communications mean power savings can reach 40%.

Other advances included new design flows with prototype simulation flow for power supply integrity, prototype flow for substrate-centred design, characterisation flow for RF validation on 65 nm, prototype chip-package co-design flow for SIP designs and prototype design for manufacturing (DfM) flow for statistical timing analysis.

As a result, designers not only benefit from an ergonomic progress thanks to integrated flows, but can also design quicker, performing simulations four times faster, extractions 30 times faster and pole/zero modelling 100 times faster. And error prevention during SRAM design makes it possible to increase yield significantly during the fabrication of circuits including a large set of such memory blocks.

ROBIN was also influential in developing a new standard for a unified chip/package data exchange (CPX) environment. Infineon and NXP have sought to push this environment, its standardised data formats and corresponding interfaces to EDA vendors. This work was carried out within the Silicon Integration Initiative (Si2) SIP working group together with LSI, Intel and IBM.

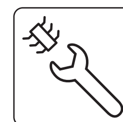
The project's industry partners are already exploiting ROBIN results to develop robust design blocks which will be used to build full-scale applications. The first users are the application-team members – post-synthesis, library and memory design – in the various design centres from Infineon, NXP and STMicroelectronics.

Important for Europe

ROBIN'S results have long-term implications for a wide variety of market applications. The SIP and network-on-chip (NOC) devices that were the focus of ROBIN will be the basis of circuit designs in applications such as digital TV power circuits, on-board intelligence in vehicles, wireless substrates used in radios and other RF circuits, multimedia platforms for mobile use, pulse-width-modulation circuitry in telecommunications and networked applications in health and medical fields.

Initial application targeted by the chipmaking partners are in digital TV, wireless and the automotive sector.

ROBIN's achievements are strategically important for the European semiconductor design and manufacturing sector. The work to improve design reliability and robustness without compromising performance will be a significant aid to European efforts in developing high-quality microelectronic devices in new 65 and 45 nm technologies.



Technology platform
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2A704: Robust design for efficient use of nanometre technologies (ROBIN)

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